Remarks

Favorable consideration of the application is respectfully requested. Claims 1-10, prior to amendment, were pending in the present application. By this paper, claims 1, 3, 4 and 5 are amended, claim 20 is added, the specification (paragraph 0029) is amended and Figures 8-10 are amended.

Support for newly added claim 20, is found in paragraph 0027 and in FIGS. 8-10. Therefore, no new matter has been added.

Claim Rejections - 35 U.S.C. §102

Claim 3, prior to this paper, was rejected under 35 U.S.C. §102(b) as being anticipated by Kamitani (U.S. Patent 6,188,115).

Claim 3 has been amended as indicated to further distinguish the present invention from Kamitani.

Claims 3:

> "said metal interconnect having a majority of a bottom surface making contact to said conductively doped active area and spanning completely between neighboring gate electrodes."

Kamitani does not disclose a metal interconnect having a majority of a bottom surface making contact to a conductively doped active area (i.e., source diffusion region) and spanning completely between neighboring gate electrodes, a feature of the present invention as relied on for amendment.

Kamitani does disclose a source electrode 43 comprising first source lines 43a (implant region) and second source lines 43b (aluminum sidewall layers). The aluminum sidewall source lines are in fact separated by silicon oxide film 15. Clearly the aluminum sidewall source lines of Kamitani do not span completely between neighboring gate electrodes.

Furthermore, the Examiner's analysis of Kamitani is clearly in error. The Examiner states that Kamitani teaches a method for forming a flash memory device on a semiconductor assembly comprising a metal interconnect 15 (referring to Figure 17 of Kamitani). Kamitani, in fact states in column 6, lines 36-38:

> "A silicon oxide film 15 serving as an interlayer isolation film is formed to cover the control gate electrodes 6."

In Kamitani, the method of forming silicon dioxide film 15 of embodiment 1 is also implemented in embodiment 4 and applied to the structure of Figure 17. Clearly, a silicon oxide film does not and cannot function as a metal interconnect.

Therefore, by amendment and by the reasons presented, the rejection of claim 3, under 35 U.S.C. §102(b) as being anticipated by Kamitani (U.S. Patent 6,188,115) is overcome.

Claim Rejections - 35 U.S.C. §103

Claims 1-2 and 4-10, prior to this paper, were rejected under 35 U.S.C. §103(a) as being unpatentable over Kamitani (U.S. Patent 6,188,115), in view of Watanabe et al. (IEDM, 98 pp. 975-978).

Claims 1, 4 and 5 have been amended as indicated to further distinguish the present invention from Kamitani in view of Watanabe et al. (hereinafter Watanabe)

Claims 1 and 5:

"forming a metal interconnect running a major length of said connected together source electrodes, said metal interconnect making a substantially continuous contact therebetween and spanning completely between neighboring gate electrodes."

Claim 4:

"forming a metal interconnect into said interconnect via, said metal interconnect running a major length of said connected together source electrodes and making contact therebetween and spanning completely between neighboring gate electrodes."

Kamitani in view of Watanabe et al. do not disclose a metal interconnect having a majority of a bottom surface making contact to a conductively doped active area (i.e., source diffusion region) and spanning completely between neighboring gate electrodes, a feature of the present invention as relied on for amendment.

Kamitani does disclose a source electrode 43 comprising first source lines 43a (implant region) and second source lines 43b (aluminum sidewall layers). The aluminum sidewall source lines 43b are in fact separated by silicon oxide film 15. Clearly the aluminum sidewall source lines of Kamitani do not span completely between neighboring gate electrodes as they are spaced apart by the presence of silicon dioxide film 15.

Furthermore, the Examiner's analysis of Kamitani is clearly in error. The Examiner states that Kamitani teaches a method for forming a flash memory device on a semiconductor assembly comprising forming a metal interconnect 15 (referring to Figure 17 of Kamitani) and forming a metal drain plug 15. Kamitani in fact states at column 6, lines 36-38:

"A silicon oxide film 15 serving as an interlayer isolation film is formed to cover the control gate electrodes 6."

In Kamitani, the method of forming silicon dioxide film 15 of embodiment 1 is also implemented in embodiment 4 and applied to the structure of Figure 17. Clearly, a silicon oxide film does not and cannot function as a metal interconnect or as a metal drain plug as stated by the Examiner.

Furthermore in Kamitani, in column 8, at lines 37 and 38 and as shown in Figure 17, conductive layer 43c is formed on drain regions 12. Figure 17 shows an insulation film 28 separating conductive layer 43c from drain regions 12. Whether conductive layer is connected to drain regions 12 certainly has not been clearly established in the disclosure of Kamitani.

Watanabe discloses on page 975:

"The number of metal sourcelines parallel to bitlines can be dramatically decreased due to low resistance of W Inter-connect compared to conventional diffused sourceline with self-aligned source structure."

Watanabe is stressing by the statement "due to low resistance of W inter-connect compared to conventional diffused sourceline with self-aligned source structure" that Watanabe is using a tungsten interconnect to each source electrode of each individual flash device **in lieu of** the conventional method of having a continuous source connection of flash devices by a diffusion source.

This point is reinforced by the illustration of Fig.1(b) of Watanabe where it is shown that the W Local Interconnect is running perpendicular to the source diffusion region and makes contact at each intersection of the source diffusion region and the W Local Interconnect.

Attempting to combine Kamitani with Watanabe, if there is in fact motivation to combine these references, will not produce the present invention as currently claimed. Kamitani does not form a metal interconnect that spans completely between neighboring gates of floating gate devices and the tungsten local interconnect of Watanabe runs perpendicular to the source diffusion of the floating gate devices and obviously does not run a major length of source electrodes connected together by a conductive implant.

Clearly, it is impossible for the combination of Kamitani and Watanabe to develop a method to form the structure of the presently claimed invention recited as:

> "forming a series of floating gate devices having their source electrodes connected together by a conductive implant into a defined active area, each source electrode being self-aligned to a respective gate electrode;
>
> forming a metal interconnect running a major length of said connected together source electrodes, said metal interconnect making a substantially continuous contact therebetween;

as presently claimed in the present invention.

Therefore, by amendment and by the reasons presented, the rejection of claims 1-2 and 4-6, under 35 U.S.C. §102(b) as being anticipated by Kamitani (U.S. Patent 6,188,115), in view of Watanabe et al. (IEDM, 98 pp. 975-978) is overcome.

The Examiner's rejection of claims 7-10 under 35 U.S.C. §103(a) as being unpatentable over Kamitani (U.S. Patent 6,188,115), in view of Watanabe et al. (IEDM, 98 pp. 975-978), is respectfully traversed.

The Examiner's analysis of Kamitani is clearly in error. The Examiner states that Kamitani teaches a method for forming a flash memory device on a semiconductor assembly comprising

forming a metal interconnect 15 (referring to Figure 17 of Kamitani) and forming a metal drain plug 15. Kamitani in fact states at column 6, lines 36-38:

> "A silicon oxide film 15 serving as an interlayer isolation film is formed to cover the control gate electrodes 6."

In Kamitani, the method of forming silicon dioxide film 15 of embodiment 1 is also implemented in embodiment 4 and applied to the structure of Figure 17. Clearly, a silicon oxide film does not and cannot function as a metal interconnect or a metal drain plug as stated by the Examiner.

Furthermore in Kamitani, in column 8, at lines 37 and 38 and as shown in Figure 17, conductive layer 43c is formed on drain regions 12. Figure 17 shows an insulation film 28 separating conductive layer 43c from drain regions 12. Whether conductive layer is connected to drain regions 12 certainly has not been clearly established in the disclosure of Kamitani.

However, Kamitani does disclose a source electrode 43 comprising first source lines 43a (implant region) and second source lines 43b (aluminum sidewall layers). The aluminum sidewall source lines are in fact separated by silicon oxide film 15. Clearly, Kamitani does not suggest replacing aluminum sidewall source lines with a tungsten-based interconnect running a major length of connected together source electrodes (by a source diffusion implant), with the tungsten-based interconnect making a substantially continuous contact to the source diffusion implant.

Watanabe discloses on page 975:

> "The number of metal sourcelines parallel to bitlines can be dramatically decreased due to low resistance of W Inter-connect compared to conventional diffused sourceline with self-aligned source structure."

Watanabe is stressing by the statement "due to low resistance of W inter-connect compared to conventional diffused sourceline with self-aligned source structure" that Watanabe is using a tungsten interconnect to each source electrode of each individual flash device **in lieu of** the conventional method of having a continuous source connection of flash devices by a diffusion source.

This point is reinforced by the illustration of Fig.1(b) of Watanabe where it is shown that the W Local Interconnect is running perpendicular to the source diffusion region and makes contact at each intersection of the source diffusion region and the W Local Interconnect.

Attempting to combine Kamitani with Watanabe, if there is in fact motivation to combine these references, will not produce the present invention as currently claimed. Kamitani does not form a metal interconnect that spans completely between neighboring gates of floating gate devices and the tungsten local interconnect of Watanabe runs perpendicular to the source diffusion of the floating gate devices and obviously does not run a major length of source electrodes connected together by a conductive implant.

Clearly, it is impossible for the combination of Kamitani and Watanabe to develop a method to form the structures of the presently claimed invention by:

> "forming a tungsten-based interconnect running a major length of said connected together source electrodes, said tungsten-based interconnect making a substantially continuous contact therebetween; and
>
> forming a tungsten-based drain plug for each floating gate device of said series of floating gate devices, said tungsten-based drain plug connecting between a drain electrode of each said floating gate device and a digit line"

as originally recited in claim 7 of the present invention, or by

"forming a tungsten-based interconnect running a major length of a series of source electrodes connected together by a conductively doped active area, said source electrodes formed in a self-aligning manner to their respective gate electrodes, said tungsten-based interconnect having a majority of a bottom surface making contact to said conductively doped active area"

as originally recited in claim 9 of the present invention, or

"forming a series of floating gate devices having their source electrodes connected together by a conductively doped active area, said source electrodes being self-aligned to their respective transistor gates of each said floating gate device;

forming a nitride barrier layer overlying each transistor gate;

forming a planarized insulation layer over said nitride barrier layer;

removing portions of said planarized insulation layer while using said nitride barrier layer to self-align an interconnect via to said source electrodes;

forming a tungsten-based interconnect into said interconnect via, said tungsten-based interconnect running a major length of said source electrodes and making contact therebetween; and

forming a tungsten-based drain plug for each floating gate device of said series of floating gate devices, said tungsten-based drain plug self-aligned to and connected between a drain electrode of each said floating gate device and a digit line"

as originally recited in claim 10 of the present invention.

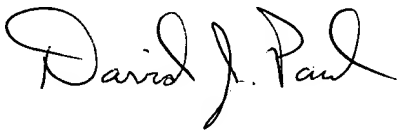
Therefore, as argued above, the rejection of claims 7-10, under 35 U.S.C. §102(b) as being anticipated by Kamitani (U.S. Patent 6,188,115), in view of Watanabe et al. (IEDM, 98 pp. 975-978) is not substantiated. It is requested that the rejection of claims 7-10, under 35 U.S.C. §102(b) as being anticipated by Kamitani (U.S. Patent 6,188,115), in view of Watanabe et al. (IEDM, 98 pp. 975-978) be withdrawn and that claims 7-10 be allowed over the art of record.

Conclusion

Applicant submits that the application is in condition for allowance. Such allowance at an early date is respectfully requested.

To that end, if the Examiner feels that a conference will expedite the prosecution of this case, the Examiner is cordially invited to call the undersigned.

Respectfully submitted,



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